O.P.Code: 23EC0403

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H.T.No.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech. II Year I Semester Regular & Supplementary Examinations November-2025

DIGITAL CIRCUITS DESIGN

Time: 3 Hours a Convert the following numbers: a Draw the circuit for 3 to 8 decoder and explain. a List out the types of number systems with one example for each b Define Multiplexer. Construct 4:1 multiplexer with logic gates and truth a Simplify the expression in S O P form using don't cares. b Perform the following subtraction by using 1's complement. g Difference between Latch and Flip-flop? List basic types of programmable logic devices. State the types of ROM. Define the following: i) Half adder and ii) Full Adder What are Universal Gates? Give their truth tables. Design a 4 bit Binary-to-BCD code converter. Write a short note on Register. What is the Sensitivity list? Differentiate between Verilog and VHDL Define Multiplexer and Demultiplexer.  $Y=\Sigma(4,5,6,8,9)+d\Sigma(3,7,10,11,14,15)$ i) 111001-1010 ii) 0011-10001 and truth table. Illustrate the digital logic gates with graphical symbol, algebraic function CO1 i) (AB)<sub>16</sub>=()<sub>2</sub> ii) (1234)<sub>8</sub>=()<sub>16</sub> (iii) (1000011)<sub>2</sub>=()<sub>10</sub> (Electronics & Communications Engineering) (Answer all the Questions  $10 \times 2 = 20 \text{ Marks}$ ) (Answer all Five Units  $5 \times 10 = 50$  Marks) DIGITAL CIRCUITS DESIGN PART-B UNIT-II I-TINU OR CO4 L2 Max. Marks: 70 C04 COS C04 C06 C06 C04 C04 COI C04 C02 C04 C01 CO4 COI L5 C01 L1 L2L3 L3 L2Ξ L2 10M 5M 5M 5M 5M 5M 5M 23 2M 2™ 2<u>M</u> 2M

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*** END ***	Comp	Draw and Briefly explain the basic structures of CPLD & FPGA.	6					:9					Deriv	Эегіу	Defin		Differ	Comp		State	Write		[(x1,	Write	What	
	are PRO			. G	н	त्य	D	С	В	Α	PS PS				e a Shift 1		entiate be	are the di		he impor	an Verilo		x2, x3)=	Verilog o	is the syr	
	Compare PROM, PLA & PLA.			a	(10)	a	9	ដ	С	2	X=0	Next State - Output	UNIT-Y  Derive the simplified sequential circuit for the following state table.		Define a Shift register and explain its types.	OR	Differentiate between synchronous and asynchronous sequential circuits.	Compare the differences between combinational and sequential circuits.	VI-TINU	State the importance of CAD Tools in HDL.	Write an Verilog code for Full Adder with the help of Truth table.		m(0, 1, 3, 4,	Write Verilog code to implement the function	tax used to v	
	LA.			0 3	f	f	f	р	d	b	X=1			UNIT-V									5, 6) using t		What is the syntax used to write a Verilog Code	
	8		OR		0	0	0	0	0	0	X:=0				es.							OR	$f(x_1, x_2, x_3) = m(0, 1, 3, 4, 5, 6)$ using the continuous assignment.			
				1	Ŧ	_		0	0	0	X=1												assignment.			
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	C05	C05											C02		C04		C04	C04		C06	C06			C06	C06	
	<b>L4</b>	L2					20						L3		L2		L2	L3		L1	L1			L1	L1	
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